Senior Design Progress Presentation

Sponsored By:

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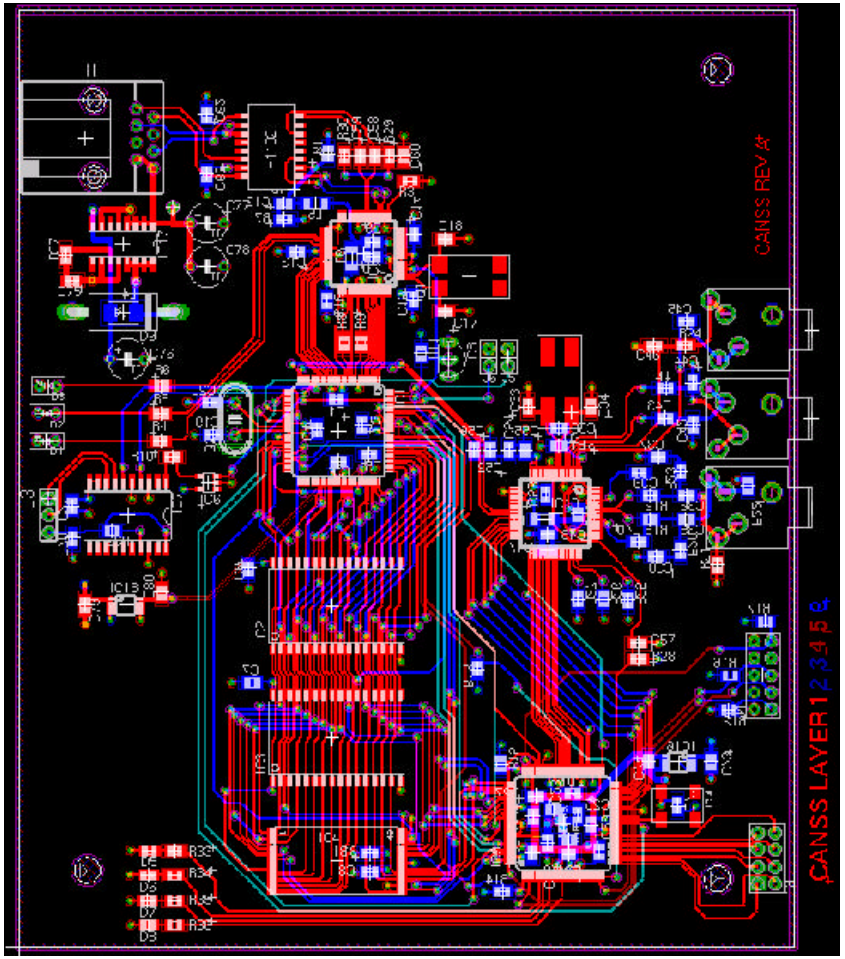
Hardware Design

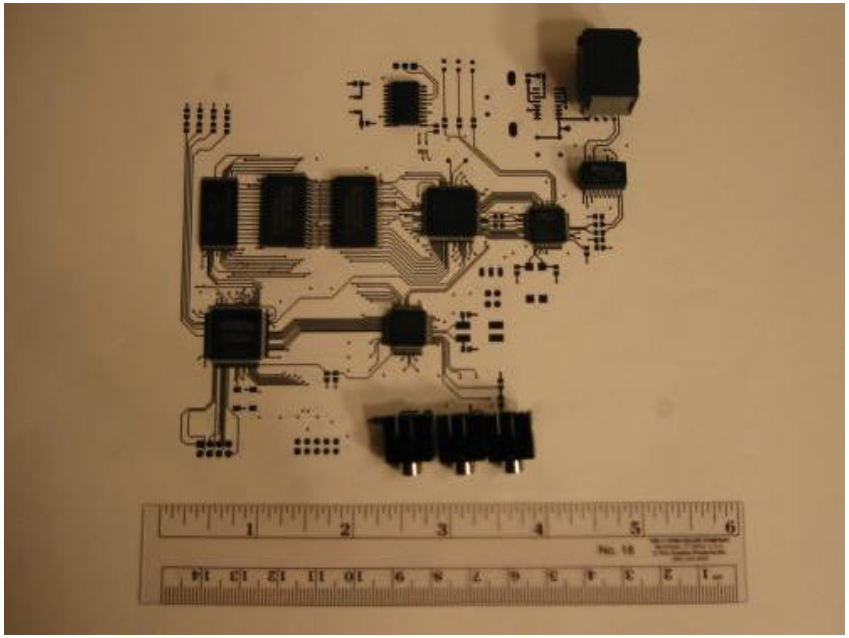
- Hardware design has been completed and the PCB is in processing at pcbexpress. Will be shipped within days.
- Overall schedule has slipped 3 weeks. The impact on software and VHDL tasks is estimated to be minimal.
- PCB Express was selected to manufacure our PCB. They provide high quality, low cost prototype boards.

Hardware Design Timeline



- Schematic Capture
  Complete 02-24-03
  Scheduled 02-14-03
- PCB Layout
  Complete 03-14-03
  Scheduled 03-06-03
- Hardware Build/Test
  Planned 04-04-03
  Scheduled 03-20-03

Hardware Design Process



PCB board paper mock-up. Final dimensions of the PCB are approximately 5x5 in.

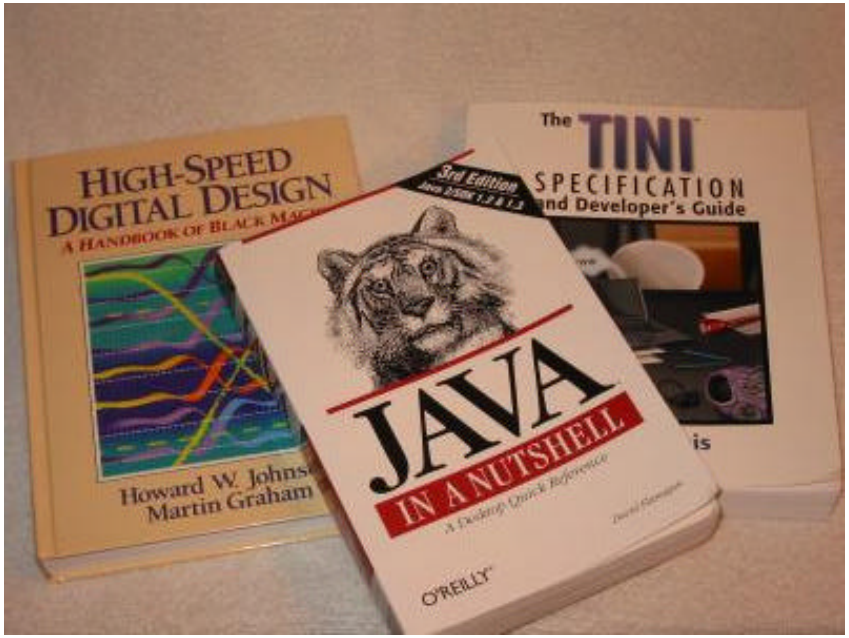
- Initial block diagrams, component selection, parts ordering
- Create Eagle (TM) library devices
- Schematic Capture
- Schematic Review
- PCB Layout
- PCB Review
- Generate manufacturing files

Accumulated Costs Thus Far

Part	Units	Cost ($)/unit	Subtotal ($)
Costs			
SRAM Memories	8	8	-$64.00
Flash	5	5	-$25.00
Micronas 3587F	3	27	-$81.00
INTEL PHI	3	7	-$21.00
FPGA	4	12	-$48.00
Dallas 80C400	3	20	-$60.00
Enclosures	3	10	-$30.00
6-layer PCB's	4		-$490.00
Misc. (Connectors, Resistors, etc.)			-$150.00
Income			
PCBexpress sponsorship			$350.00
IEEE Project Fund (expected)			$300.00
TOTAL ($)			-$319.00

- Total costs have been minimized by utilizing sample parts when available
- The single largest cost item is the PCB. The decision to use a more expensive six-layer board was motivated by two main factors: trace impedance and ease of routing.
- Production costs would be significantly less due to mass production.

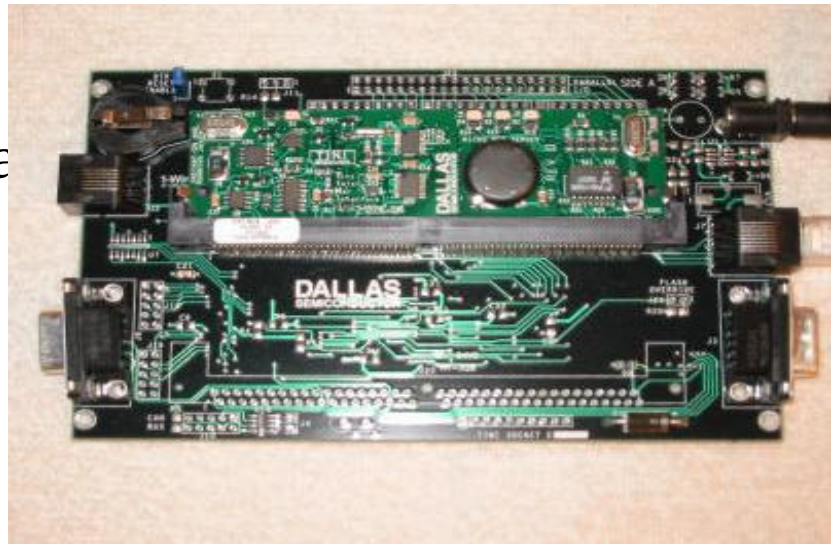
What's Next For Hardware?



- Build 3 CANSS boards
- Write hardware checkout VHDL
- Write software to load FPGA
- Write hardware checkout software

Software Design

- TINI Java development environment installed and configured.
- Connectivity with TINI developer boa established and tested with “Hello World” program.
- New UML tool, “Umbrello”, being utilized in the software design phase.
- JDK 1.4 “Vector” and “Thread” classes being used for shared buffering and semaphore locking in inter-thread communications.



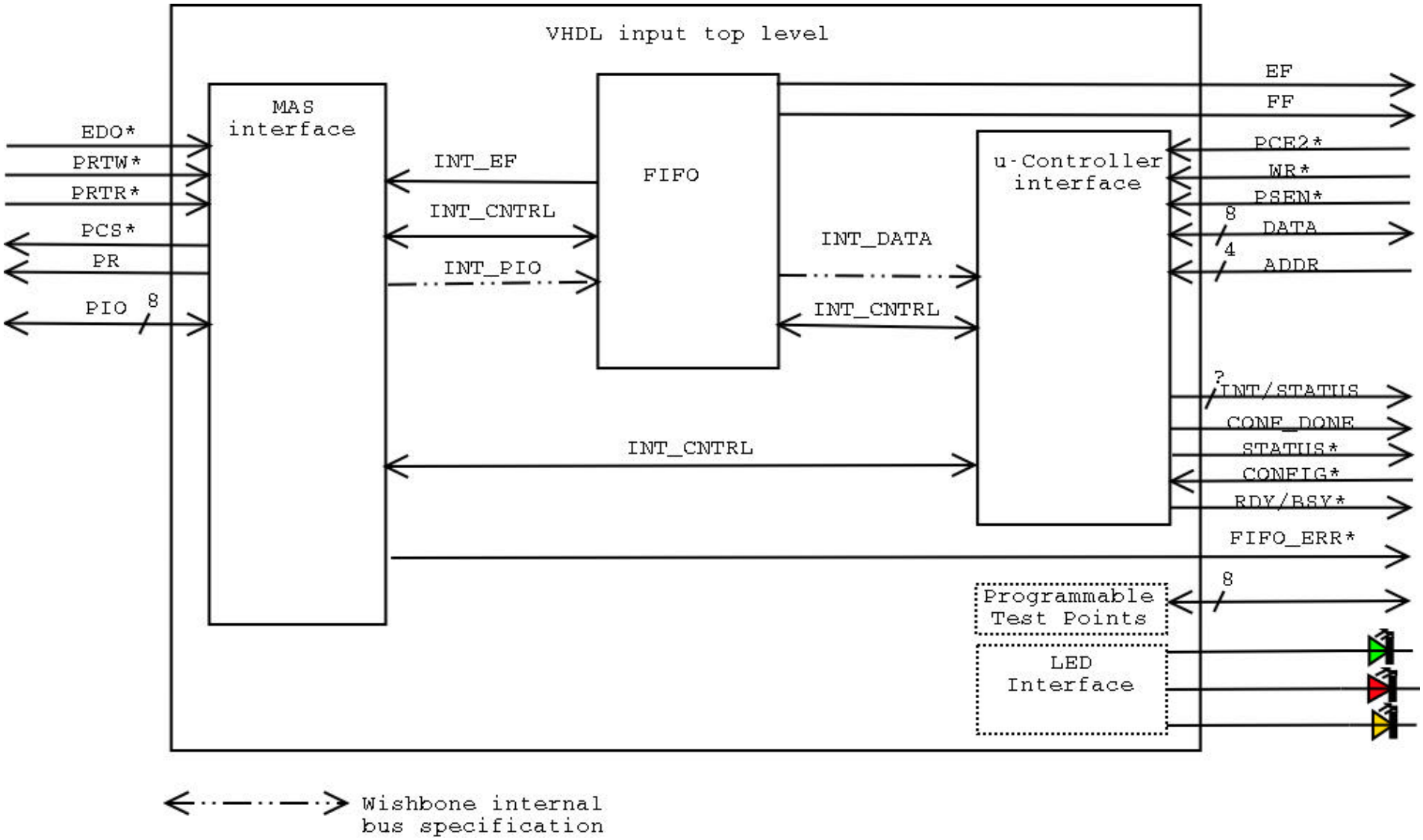
Software Design Schedule

- Several weeks behind original schedule
- Umbrello UML modeling software will accelerate the coding process, as it can create Java “framework” code from UML diagrams
- Pre-existing JDK 1.4 “Vector” class will help greatly with buffering techniques and data integrity/locking issues, speeding up the design process
- Upcoming software challenges: throughput and buffering issues, the “FPGA programming” class, integration with new hardware, and network configuration/control design and implementation

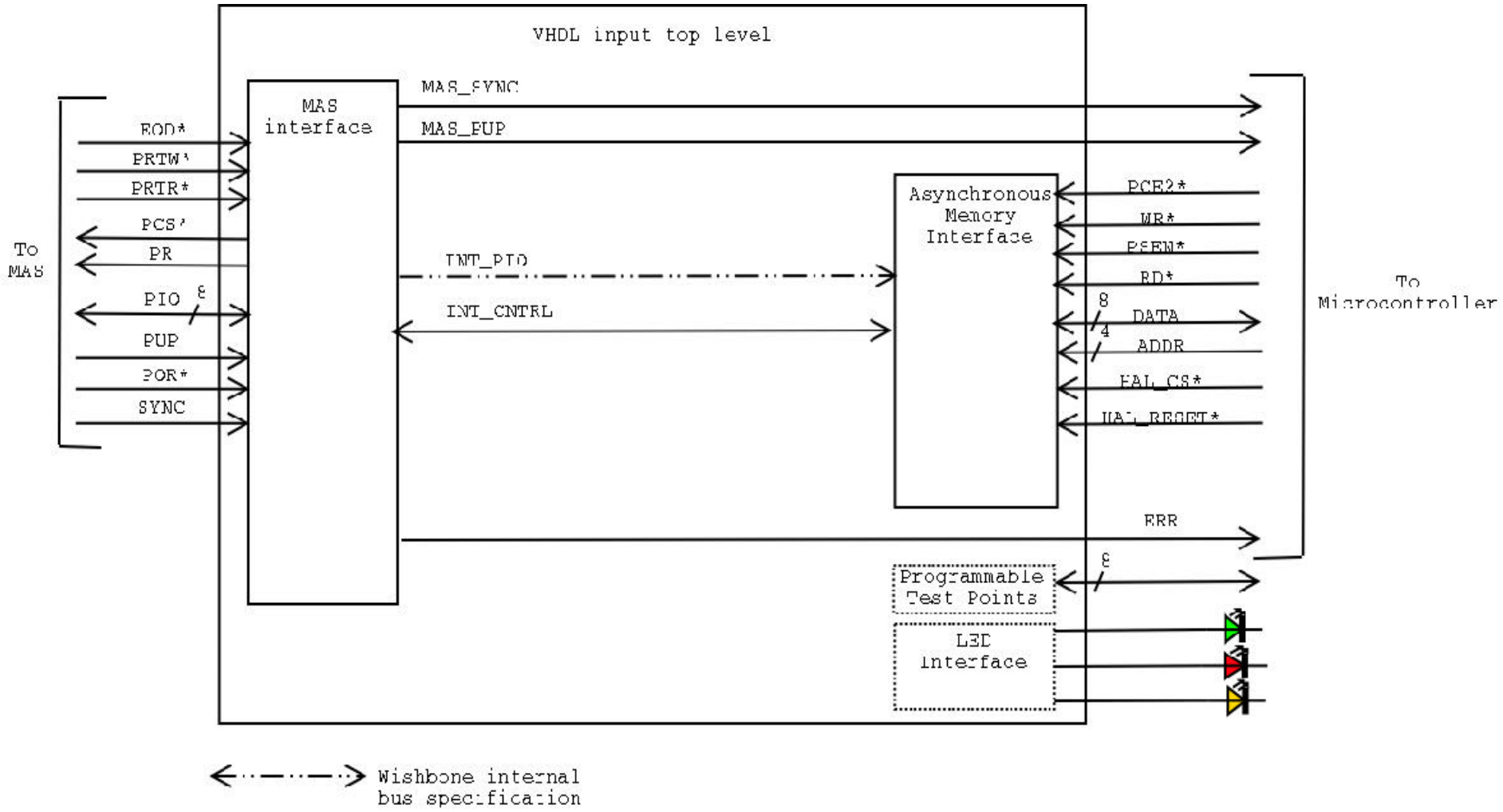
VHDL Design

- Three weeks behind schedule
- Created a simplified architecture without a FIFO to implement initially
- A simplified MAS interface and testbench entities are ready for simfulation
- Started Asynchronous Memory Interface entity

Initial VHDL Design



Simplified VHDL Design



Conclusions/Useful Links

QUESTIONS?? COMMENTS?? NEED A BEER??

- CANSS homepage - canss.dhs.org
- PCB Express - www.pcbexpress.com
- Eagle - www.cadsoft.de
- Umbrello - uml.sourceforge.net